V3208D
2048-Stage Low Voltage Operation Low Noise BBD

Product Specification

1、General Description

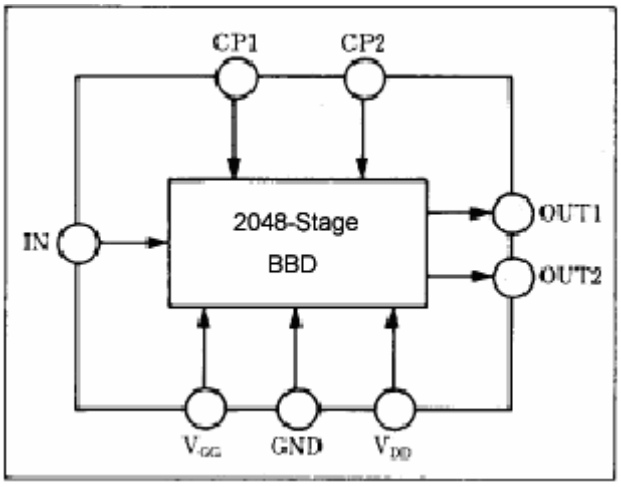
The V3208D is a 2048-stage low voltage operation (VDD = 5V) BBD that provides a signal delay of up to 102.4ms at clock frequency 10KHz and is suitable for use as reverberation effect of audio equipments such as portable stereo and radio cassette recorders which need low voltage and long delay time since S/N is 71dB in spite of many stages.

Features:

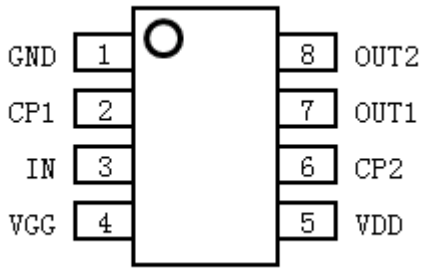
- Variable delay of audio signals: 10.24ms ~ 102.4ms.
- Wide power supply voltage: 4 ~ 10V.
- No insertion loss: Li = 0dB typ.
- Wide dynamic range: S/N = 71dB.
- N Channel silicon gate process.
- DIP8

2、Block Diagram And Pin Description

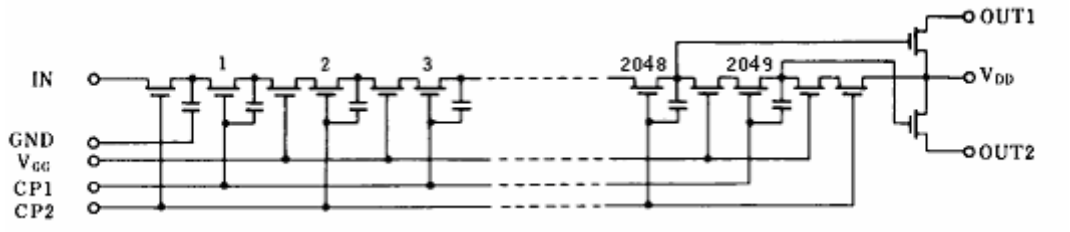
2.1、Block Diagram



2.2、Pin Configurations



2.3、Circuit Diagram



2.4、Pin Description

Pin No.	Pin Name	Description
1	GND	Ground
2	CP1	The first clock input
3	IN	Analog signal input
4	VGG	Bias voltage input ($14/15V_{DD}$)
5	VDD	Power
6	CP2	The second clock input
7	OUT1	Signal output, delayed 4096 times
8	OUT2	Signal output, delayed 4097 times

3、Electrical Parameter

3.1、 Absolute Maximum Ratings

(Tamb=25℃, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Min.	Max.	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_i	-0.3	11	V
Output Voltage	V_O	-0.3	11	V
Operation Ambient Temp.	T_{opr}	-20	60	℃
Storage Temp.	T_{stg}	-55	125	℃
Soldering Temp	T_L		245	℃

3.2、 Operating Condition

(Tamb=25℃ , V_{DD}=5V, unless otherwise specified)

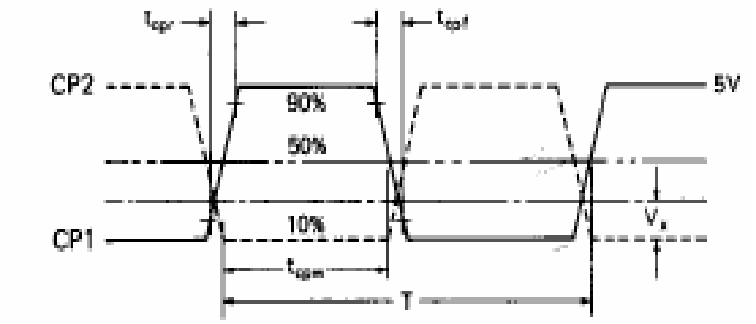
Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	4	5	10	V
Gate Supply Voltage	V_{GG}		$14/15V_{DD}$		V
Clock Voltage High	Vcph		V_{DD}		V
Clock Voltage Low	Vcpl	0		+0.5	V
Clock frequency	Fcp	10		100	KHz
Clock Pulse Width	Tcpw			0.5T	
Clock Rise Time	Tcpr			500	Ns
Clock fall Time	Tcpf			500	Ns
Clock Input Cap.	Ccp			2800	Pf
Clock Cross Point	Vx	0		$0.3V_{CPH}$	v

3.3、 Electrical Characteristics

(**Ta = 25**℃, $V_{DD} = V_{CPH} = 5V$, $V_{CPL} = 0V$, $V_{GG} = {}^{14}/_{15}\, V_{DD}$, R_L=100kΩ)

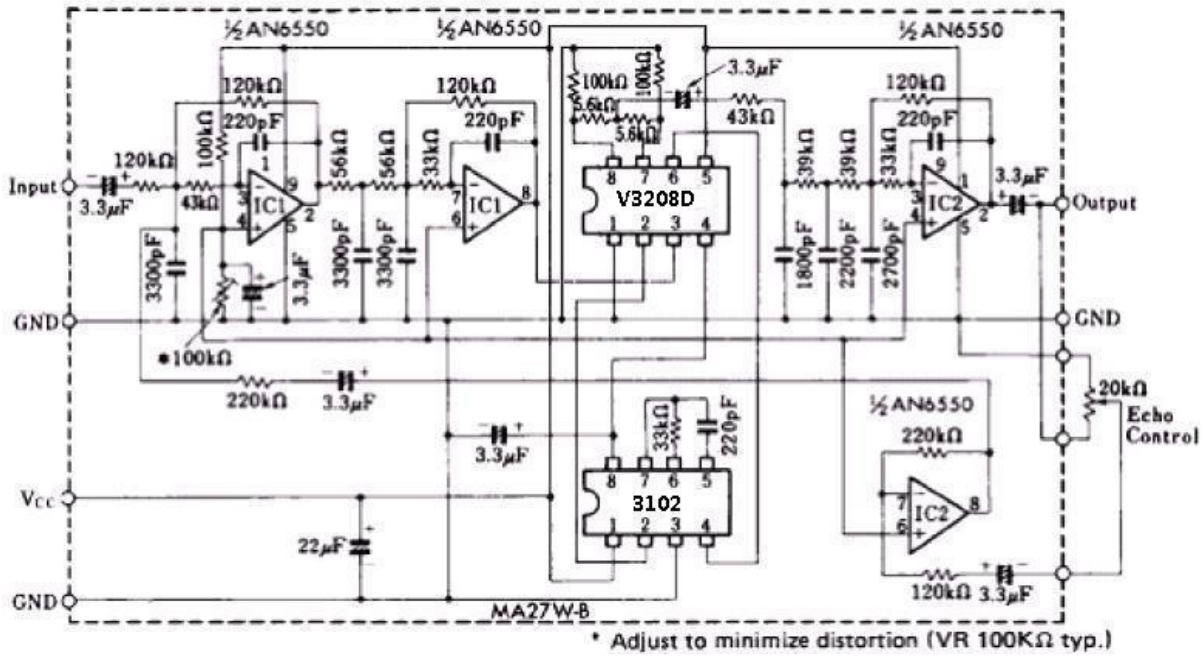
Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal Delay time	td	10.24		102.4	Ms
Input Signal Freq. fcp= 40kHz, Output Attenuation ≤ 3dB	fi	10			kHz
Input Signal Swing THD = 2.5%	Vi		0.36		Vrms
Insertion Loss fcp = 40kHz, fi= 1kHz	Li	-4	0	4	dB
Total Harm. Dist. fcp = 40kHz, fi = 1kHz, Vi= 0.25 Vrms	THD		0.8	2.5	%
Output Noise Voltage fcp = 100 kHz, Weighted by "A" curve	Vno			0.25	mVrms
Signal to Noise Ratio fcp= 100 kHz, Weighted by "A" curve	S/N		71		dB

3.4、Clock Pulse Waveform



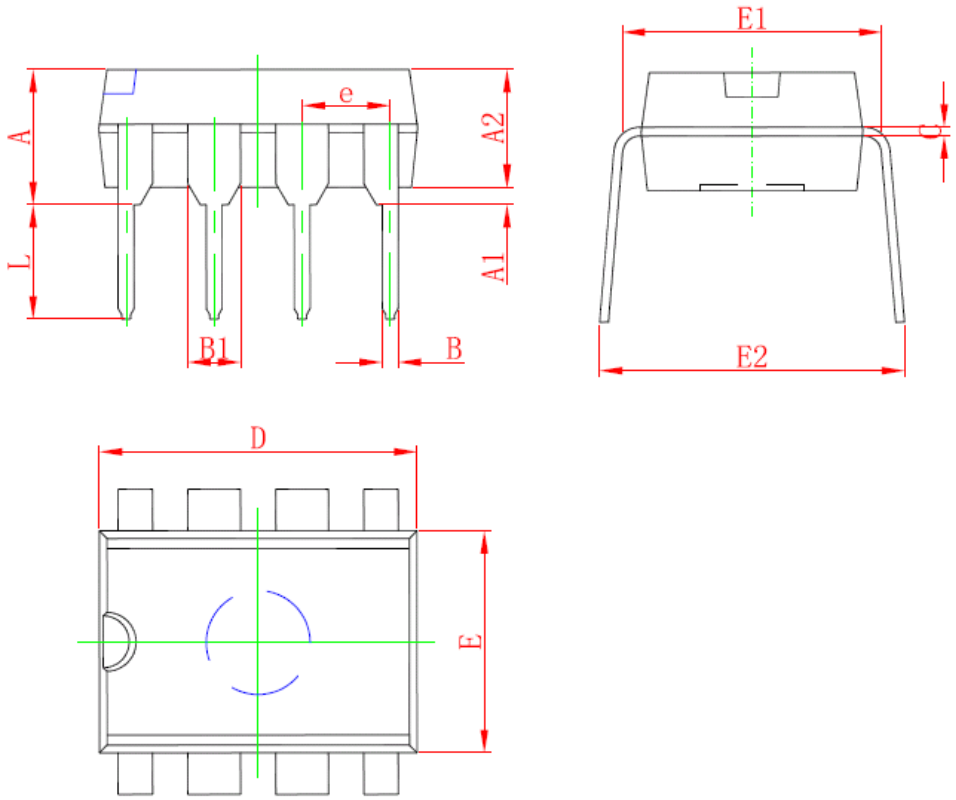
$T = 1/f_{CP}$ (Clock Period)

4、Typical Application Circuit



5、Package Information

5.1、DIP8 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354